07-12-00 A

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Mathew A Rybicki et al.

Docket No. SIG000030

Title: METHOD AND APPARATUS FOR PROVIDING MULTIPLE CHANNEL AUDIO IN A COMPUTING SYSTEM

Date: 7/10/2000

To the Honorable Commissioner
of Patents and Trademarks
Box Patent Application
Washington, D.C. 20231

REQUEST FOR FILING A NATIONAL PATENT APPLICATION

The applicants respectfully requestthat the above captioned patent application be accepted for examination. This patent application is a:

- [X] new patent application
- [ ] continuation in part (CIP) of Application Serial No. [ ] filed on [ ]
- [ ] divisional application of Application Serial No. [ ] filed on [ ]
- [ ] continuation application of Application Serial No. [ ] filed on [ ]

Accompanying this request is (as indicated by an "X" in the corresponding box):

- [X] 1. 18 pages of specification, which includes the claims and abstract, and 4 sheets of formal drawings;
- [X] 2. Combined Declaration and Power of Attorney;
- [ ] 3. An Information Disclosure Statement along with the references;
- [ ] 4. A petition to extend the response for a priority application identified above;
- [X] 5. An assignment assigning all rights in the above referenced patent application to SigmaTel, Inc.;
- [X] 6. An assignment recording cover sheet;
- [X] 7. A verified statement establishing small entity status under 37 C.F.R. Sections 1.9 and 1.27;
- [X] 8. A certificate of mailing indicating that the above captioned patent application has been deposited as "Express Mail" with the United States Postal Service;
- [ ] 9. A certificate of mailing indicating that the above captioned patent application has been deposited with the United States Postal Service with sufficient postage as first class mail;
- [X] 10. A return postcard; and
- [ ] 11. A preliminary amendment.

The filing fee for the above captioned patent application is as follows:

Large entity status apply? [no]

				basic filing fee	345.00
total claims	24	extra per claim fee	9.00	extra claim fee	36.00
total ind claims	6	extra per ind claim fee	39.00	extra ind claim fee	117.00
				assign record fee	40.00
				TOTAL FILING FEE	538.00

Payment of the above calculated filing fee is as follows (as indicated by the "X" in the corresponding box):

[X] A check in the amount of $ 538.00

[ ] Please charge Deposit Account No. in the amount of $

A duplicate sheet is attached.

Respectfully submitted,

By: _____

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Registration No: 33,534
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SIG000030

Customer No: 000024263
SigmaTel, Inc.,
2700 Via Fortuna, Suite 500
Austin, Texas 78746

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Mathew A Rybicki et al. Examiner:

Serial No. Art Group:

Filing Date: Docket No. SIG000030

Title: METHOD AND APPARATUS FOR PROVIDING MULTIPLE CHANNEL AUDIO IN A COMPUTING SYSTEM

7/7/2000

To the Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF EXPRESS MAILING

Express Mail Label EL581298055US Name of Depositor: Diane Hudson

Date of Deposit: 7/10/00 Signature: Diane Hudson

I hereby certify that this paper and the items identified below are being deposited with the U.S. Postal Service "Express Mail Post Office to Addresses" service under 37 C.F.R. Section 1.10 on the 'Date of Deposit', indicated above, and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Items accompanying this Certificate of Express Mailing:

- [X] 1. A new patent application including 18 pages of specification, and 4 sheets of formal drawings;
- [X] 2. Combined Declaration and Power of Attorney;
- [ ] 3. An Information Disclosure Statement along with the references;
- [ ] 4. A petition to extend the response for a priority application identified above;
- [X] 5. An assignment assigning all rights in the above referenced patent application to SigmaTel, Inc.;
- [X] 6. An assignment recording cover sheet;
- [X] 7. A verified statement establishing small entity status under 37 C.F.R. Sections 1.9 and 1.27;
- [X] 8. A return postcard; and
- [ ] 9. A preliminary amendment.

SigmaTel, Inc.
Customer No: 000024263

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Mathew A Rybicki et al. Examiner:

Serial No. Art Group:

Filing Date: Docket No. SIG000030

Title: METHOD AND APPARATUS FOR PROVIDING MULTIPLE CHANNEL AUDIO IN A COMPUTING SYSTEM

7/10/2000

To the Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

STATEMENT OF STATUS AS SMALL ENTITY
Pursuant to 37 C.F.R. Section 1.27 and Section 1.9

For the above captioned patent application, a party in interest avers that it qualifies for small entity status as SMALL BUSINESS CONCERN. To verify the small entity status, the party in interest attests that:

1. This verified statement for the above captioned patent application or patent is being submitted prior to or with the first fee paid as a small entity;

2. For purposes of this verified statement, as defined in 37 C.F.R. Section 1.27, a license to a Federal agency resulting from a funding agreement with that agency pursuant to 35 U.S.C. 202 (c) (4) does not constitute a license.

3. As a SMALL BUSINESS CONCERN:
(a) I swear that I am an official of SigmaTel, Inc., empowered to act on behalf of SigmaTel, Inc.,
(b) In my capacity as identified in this section 3(a), I swear that SigmaTel, Inc. qualifies as a small business concern as defined in 37 C.F.R Section 1.9 and that the number of employees of SigmaTel, Inc. and those of its affiliates, does not exceed 500 persons;
(c) I further swear that my signature appears at the end of this Statement of Status as Small Entity;
(d) I still further swear that, in support my of contention that SigmaTel, Inc. qualifies as a small business concern, exclusive rights to the invention of the above captioned patent application have been conveyed to and remain with SigmaTel, Inc.,

Signatures of Person(s) Making the Verified Statement

SigmaTel, Inc. (Customer No:000024263)
Name: Timothy W. Markison

Signature Date 7/10/00
Title: General Counsel

METHOD AND APPARTUS FOR PROVIDING MULTIPLE CHANNEL AUDIO IN A COMPUTING SYSTEM

TECHNICAL FIRLD OF THE INVENTION

This invention relates generally to computers and more particularly to audio processing in computers.

BACKGROUND OF THE INVENTION

As is known, personal computers (PC) and laptop computers include audio processing circuitry. Such audio processing circuitry allows a computer to play CDs, DVDs, etc. and produce audible sound therefrom. Current PCs and laptop computers include three audio jacks to facilitate the processing of audio. The three audio jacks are typically labeled line-in, microphone, and line-out. The line-in audio jack is used to receive analog audio signals from external devices, such as a CD player, cassette player, etc. The audio processing circuitry receives the analog audio signals via the line-in audio jack and converts the analog signals into digital signals, which can be manipulated by the computer. The audio processing circuitry also receives digital audio signals from the computer, converts them to analog signals, and provides the analog signals to speakers via the line-out audio jack. The digital audio signals may result from playback of a CD via an internal CD driver, mixed digital audio, etc. The audio processing circuitry may also receive analog audio signals via the microphone audio jack and convert these analog audio signals into digital audio signals for processing by the computer.

With advances in audio processing circuitry, surround-sound and other audio effects are readily available. For example, three-dimensional audio, audio synthesis via a wave table, pitch alterations, echo, etc. However, in the PC and laptop computing environments, such computing

devices only include three audio jacks (line-in, line-out, and microphone). As such, current PC and laptop devices only accommodate stereo audio and not multi-channel or surround-sound audio.

Therefore, a need exists for a method and apparatus that provides multi-channel audio in a computing system.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a schematic block diagram of a soundcard or motherboard that includes circuitry for providing multiple channel audio in a computing system in accordance with the present invention;

Figure 2 illustrates a schematic block diagram of an alternate soundcard or motherboard that includes circuitry for providing multiple channel audio in a computing system in accordance with the present invention;

Figure 3 illustrates a schematic block diagram of an audio codec that provides multiple channel audio in a computing system in accordance with the present invention;

Figure 4 illustrates a schematic block diagram of an audio codec in accordance with the present invention;

Figure 5 illustrates a logic diagram of a method for providing multiple channel audio in a computing system in accordance with the present invention; and

Figure 6 illustrates a logic diagram of an alternate method for providing multiple channel audio in a computing system in accordance with the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Generally, the present invention provides a method and apparatus for providing multiple channel audio in a computing system. Such a method and apparatus includes processing that begins by receiving an audio setup signal that indicates whether audio is to be outputted as stereo audio or multiple channel audio. When multiple channel audio is to be outputted, the line-in driver is disabled in the audio processing circuitry and the multiple channel driver of the audio processing circuitry is enabled. Thus, the multiple channel driver is operably coupled to the line-in audio jack. When the audio output is to be outputted as stereo audio, the multiple channel driver is disabled and the line-in driver is enable. Thus, the line-in driver is operably coupled to the line-in audio jack. With such a method and apparatus, multiple channel audio may be provided in a personal computer and/or laptop utilizing the existing three audio jacks.

The present inventions then were fully described with reference to Figures 1 through 6. Figure 1 illustrates a schematic block diagram of a soundcard or motherboard 10 that includes a controller 12 and an audio codec 14. The soundcard or motherboard 10 is included in a personal computer, a laptop computer or other computing device that includes user audio inputs via audio jacks labeled line-in 16, microphone in 18 and line-out 20, or the equivalent thereof. The controller 12 may be an integrated digital controller or a software controller. The integrated digital controller is typically an integrated circuit that is mounted on the soundcard or the motherboard. A software controller is stored in system memory and executed by the central processing unit of the computer. In either implementation, the controller 12 provides an interface between the central processing unit and the audio codec 14. For example, if the audio processing is done in accordance with the AC 97 Specification, the controller 12 will function in accordance with the AC 97 Specification.

In AC97 applications, the controller communicates digitized audio data 36 with the audio codec 14. The digitized audio data 36 includes audio data and control data. The audio data includes left channel audio data, right channel audio data and, for multiple channel audio, left rear channel audio data, and right rear channel audio data. The control data indicates audio set-up data and other

control data as specified in the AC97 Specification. The audio set-up data indicates whether the audio output is to be processed as stereo audio (i.e. only utilizing the left and right audio data) or multi-channel output (i.e. utilizing rear left and right audio data and the front left and right audio data).

The audio codec 14 includes the audio setting register 22, an input/output (I/O) interface 26, audio codec processing circuitry 24, a line-in driver 28 that includes left and right drivers, a multi-channel driver 30 that includes left and right drivers, a microphone driver 32, and a line-out driver 34 that includes left and right drivers. The audio codec processing circuitry 24 may be similar to the circuitry found in audio codecs produced and manufactured by SigmaTel, Inc. For example, the STAC 9708 designed and manufactured by SigmaTel, Inc. would include the circuitry contained in the audio codec processing circuitry 24.

In an AC97 Specification compliant system, the I/O interface 26 of the audio codec 14 communicates with the controller 12 via the AC link. The I/O interface 26 provides the audio data of the digitized audio data 36 to the audio codec processing circuitry 24 and provides the audio setup signal, or audio setting information 38, to the audio setting register 22. If the audio setting information 38 indicates that stereo operation is to be performed, the multi-channel driver 30 is disabled and the line-in driver 28 is enabled such that only the line-in driver 28 in operably coupled to the line-in audio jack 16. In this embodiment, the performance of the audio codec processing circuitry 24 with respect to the microphone driver 32 and line-out driver 34 is known.

When the audio setting information 38 indicates that multiple channel audio is to be implemented, line-in driver 28 is disabled and the multiple channel driver 30 is enabled. When multiple channel driver 30 is enabled, it is coupled to the line-in audio jack 16. When coupled in this manner, the line-in audio jack 16 is used as an output audio jack for providing the left and right rear audio signals to left and right rear speakers of a multi-channel audio system. In this configuration, a PC or laptop may provide surround sound audio without deviating from the current three audio jack implementation.

Figure 2 illustrates an alternate sound card or motherboard 40, which includes the controller 12 and the audio codec 14. In this configuration, however, the microphone input audio jack 18 is used in a dual mode as opposed to the line-in audio jack 16. As such, when the audio setting information 38 indicates stereo operation, the multi-channel driver 30 is disabled and the microphone driver 32 is enabled such that only the microphone driver 32 is operably coupled to the microphone audio jack 18. Conversely, when the audio setting information 38 indicates multiple channel audio, the microphone driver 32 is disabled and the multiple channel driver 30 is enabled. When coupled in this manner, the microphone audio jack 18 is used as an output audio jack for providing the left and right rear audio signals to left and right rear speakers of a multi-channel audio system.

Figure 3 illustrates a detailed schematic block diagram of a portion of the audio codec 14. As shown, the multiple channel driver 30 includes a left channel driver 58 and a right channel driver 60, the audio setting register 22 includes a line-in register 50 and a multi-channel register 52, and the line-in driver 28 includes a right channel driver and a left channel driver. The left and right drivers of the line-in driver 28 are capacitively coupled to the line-in audio jack 16 as are the left and right drivers 58 and 60 of the multi-channel driver 30.

The audio setup signal, or audio setting information 38, includes mute/unmute information 54 and stereo/multi-channel operation information 56, which are stored in the line-in register 50 and the multiple channel register 52, respectively, of the audio setting register 22. When stereo operation is indicated, the mute/unmute signal indicates unmute mode while the stereo/multi-channel operation 56 indicates stereo mode. Conversely, when multi-channel operation is indicated, the mute/unmute signal indicates mute mode while the stereo/multi-channel operation 56 indicates multi-channel mode.

The multiple channel driver 30 further includes 3-D audio circuitry and a disabling circuit 62. The 3-D audio circuitry includes a resistive network and switching elements. In operation, the 3-D is enabled when the 3-D on switches are activated and the 3-D off switches are deactivate such that the outputs of the left channel driver 58 and right channel driver 60 are cross-coupled via the resistive

network. When the 3-D is disabled, the 3-D off switches are enabled and the 3-D on switches are disabled such that the left and right channel drivers 58 and 60 operate as buffers.

The disabling circuit 62 includes a pair of drivers coupled to a reference potential within the audio codec 14. In operation, the disabling circuit switches are closed such that the center points of the resistive networks of the 3-D audio circuitry are coupled to the reference potential. This prevents cross coupling of the line-in signals via the resistive network and keeps the left side of the rear output capacitors biased to prevent turn on popping sounds. In addition, the left and right channel drivers 58 and 60 may be placed in a high impedance state. When multiple channel operation is indicated, the switches of the disabling circuit are opened thereby allowing the multiple channel driver 30 to provide surround sound audio signals to the line-in audio jack 16. In addition, the line-in driver 28 is placed in a mute state. Note that if the audio codec 14 does not include the 3-D audio circuitry, the disabling circuit would include a resistor coupled from each rear output and to bias the capacitors.

Figure 4 illustrates a schematic block diagram of an audio codec 70 that includes a processing module 72 and memory 74. The processing module 72 may be a single processing device or a plurality of processing devices. Such a processing device may be a microprocessor, microcontroller, digital signal processor, state machine, logic circuitry, and/or any device that processes signals (e.g. analog or digital) based on operational instructions. The memory 74 may be a single memory device or a plurality of memory devices. Such a memory device may be read only memory, random access memory, flash memory, system memory, and/or any device that stores digital information. Note that when the processing module 72 implements one or more of its functions via a state machine or logic circuitry, the memory storing the corresponding operational instructions is imbedded within the circuitry comprising the state machine and logic circuitry. The operational instructions stored in memory 74 and executed by processing module 72 are illustrated in Figures 5 and 6.

Figure 5 illustrates a logic diagram of a method for providing multiple channel audio in a computing system. The process begins at Step 80 where an audio setup signal is received, wherein the audio setup signal indicates whether stereo audio or multiple channel audio is to be processed. The process then proceeds to Step 82 where a determination is made as to whether the audio is to be

outputted as stereo audio or as multiple channel audio. Note that the determination is made based on a user selection, auto detection of speakers coupled to an input jack, or sensing the coupling of the audio jacks. When the audio is to be outputted as multiple channel audio, the process proceeds to Step 84 where a line-in driver is disabled such that a multiple channel driver is operably coupled to the line-in audio jack. If, however, the audio is to be outputted as stereo audio, the process proceeds to Step 86. At Step 86, a multiple channel driver is disabled such that a line-in driver is operably coupled to the line-in audio jack.

Figure 6 illustrates an alternate method that begins at Step 90 where an audio setup signal that indicates stereo audio operation or multiple channel audio operation is received. The process then proceeds to Step 92 where a determination is made as to whether audio is to be outputted as stereo audio or multiple channel audio. When the audio is to be outputted as multiple channel audio, the process proceeds to Step 94. At Step 94 a microphone driver is disabled such that a multiple channel driver is operably coupled to the microphone audio jack. If, however, stereo audio is to be outputted the process proceeds to Step 96. At Step 96, a multiple channel driver is disabled such that a microphone driver is operably coupled to the microphone audio jack.

The preceding discussion has presented a method and apparatus for providing multi-channel audio in a computing system such as a personal computer or laptop computer. By including in the audio codec circuitry to switch between stereo and multiple channel audio, a personal computer or laptop can readily provide multiple channel audio. As one of average skill in the art will appreciate, other embodiments may be derived from the teaching of the present invention without deviating from the scope of the claims.

CLAIMS

What is claimed is:

1. A method for providing multiple channel audio in a computing system, the method comprises the steps of:

receiving an audio setup signal that indicates whether audio is to be outputted as stereo audio or multiple channel audio;

when the multiple channel audio is to be outputted, disabling a line-in driver such that a multiple channel driver is operably coupled to an audio jack; and

when the stereo audio is to be outputted, disabling the multiple channel driver such that the line-in driver is operably coupled to the audio jack.

2. The method of claim 1, wherein the step of receiving the audio setup signal further comprises:

receiving line-in driver setting information and multiple channel driver setting information;

storing the line-in driver setting information in a line-in driver register; and

storing the multiple channel driver setting information in a multiple channel register.

3. The method of claim 1, wherein the disabling the line-in driver further comprises muting the line-in driver.

4. The method of claim 1, wherein the disabling the multiple channel driver further comprises placing the multiple channel driver in a high impedance state.

5. An audio codec comprising:

an input/output interface operably coupled to receive and transmit digitized audio data;

an audio setting register that stores audio setting information contained in the digitized audio data;

a line-in driver operably coupled to an external audio jack when the audio setting information indicates stereo audio operation and is disabled when the audio setting information indicates multiple channel audio operation; and

a multiple channel driver operably coupled to the external audio jack when the audio setting information indicates multiple channel audio operation and is disabled when the audio setting information indicates stereo audio operation

6. The audio codec of claim 5, wherein the audio setting register further comprises:

multiple channel register that stores multiple channel setting information of the audio setting information; and

a line-in register that stores line-in setting information of the audio setting information.

7. The audio codec of claim 5, wherein the multiple channel driver further comprises:

a left channel driver;

a right channel driver; and

a disabling circuit operably coupled to the left channel driver and the right channel driver, wherein the disabling circuit disables the left channel driver and the right channel driver when the audio setting information indicates stereo operation.

8. The audio codec of claim 7, wherein the disabling circuit causes the left and right channel drivers to have a high impedance with respect to the external audio jack when the audio setting information indicates the stereo operation.

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9. An audio codec comprises:

a processing module; and

memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

receive an audio setup signal that indicates whether audio is to be outputted as stereo audio or multiple channel audio;

when the multiple channel audio is to be outputted, disable a line-in driver such that a multiple channel driver is operably coupled to an audio jack; and

when the stereo audio is to be outputted, disable the multiple channel driver such that the line-in driver is operably coupled to the audio jack.

10. The audio codec of claim 9, wherein the memory further comprises operational instructions that cause the processing to receive the audio setup signal by:

receiving line-in driver setting information and multiple channel driver setting information;

storing the line-in driver setting information in a line driver register; and

storing the multiple channel driver setting information in a multiple channel register.

11. The audio codec of claim 9, wherein the memory further comprises operational instructions that cause the processing to disable the line-in driver by muting the line driver.

12. The audio codec of claim 9, wherein the memory further comprises operational instructions that cause the processing to disable the multiple channel driver by placing the multiple channel driver in a high impedance state.

13. A method for providing multiple channel audio in a computing system, the method comprises the steps of:

receiving an audio setup signal that indicates whether audio is to be outputted as stereo audio or multiple channel audio;

when the multiple channel audio is to be outputted, disabling a microphone driver such that a multiple channel driver is operably coupled to an audio jack; and

when the stereo audio is to be outputted, disabling the multiple channel driver such that the microphone driver is operably coupled to the audio jack.

14. The method of claim 13, wherein the step of receiving the audio setup signal further comprises:

receiving microphone driver setting information and multiple channel driver setting information;

storing the microphone driver setting information in a microphone driver register; and

storing the multiple channel driver setting information in a multiple channel register.

15. The method of claim 13, wherein the disabling the microphone driver further comprises muting the microphone.

16. The method of claim 13, wherein the disabling the multiple channel driver further comprises placing the multiple channel driver in a high impedance state.

17. An audio codec comprising:

an input/output interface operably coupled to receive and transmit audio data;

an audio setting register that stores audio setting information contained in the audio data;

a microphone driver operably coupled to an external audio jack when the audio setting information indicates stereo audio operation and is disabled when the audio setting information indicates multiple channel audio operation; and

a multiple channel driver operably coupled to the external audio jack when the audio setting information indicates multiple channel audio operation and is disabled when the audio setting information indicates stereo audio operation

18. The audio codec of claim 17, wherein the audio setting register further comprises:

multiple channel register that stores multiple channel setting information of the audio setting information; and

a microphone register that stores microphone setting information of the audio setting information.

19. The audio codec of claim 17, wherein the multiple channel driver further comprises:

a left channel driver;

a right channel driver; and

a disabling circuit operably coupled to the left channel driver and the right channel driver, wherein the disabling circuit disables the left channel driver and the right channel driver when the audio setting information indicates stereo operation.

20. The audio codec of claim 19, wherein the disabling circuit causes the left and right channel drivers to have a high impedance with respect to the external audio jack when the audio setting information indicates the stereo operation.

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21. An audio codec comprises:

a processing module; and

memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

receive an audio setup signal that indicates whether audio is to be outputted as stereo audio or multiple channel audio;

when the multiple channel audio is to be outputted, disable a microphone driver such that a multiple channel driver is operably coupled to an audio jack; and

when the stereo audio is to be outputted, disable the multiple channel driver such that the microphone driver is operably coupled to the audio jack.

22. The audio codec of claim 21, wherein the memory further comprises operational instructions that cause the processing to receive the audio setup signal by:

receiving microphone driver setting information and multiple channel driver setting information;

storing the microphone driver setting information in a line driver register; and

storing the multiple channel driver setting information in a multiple channel register.

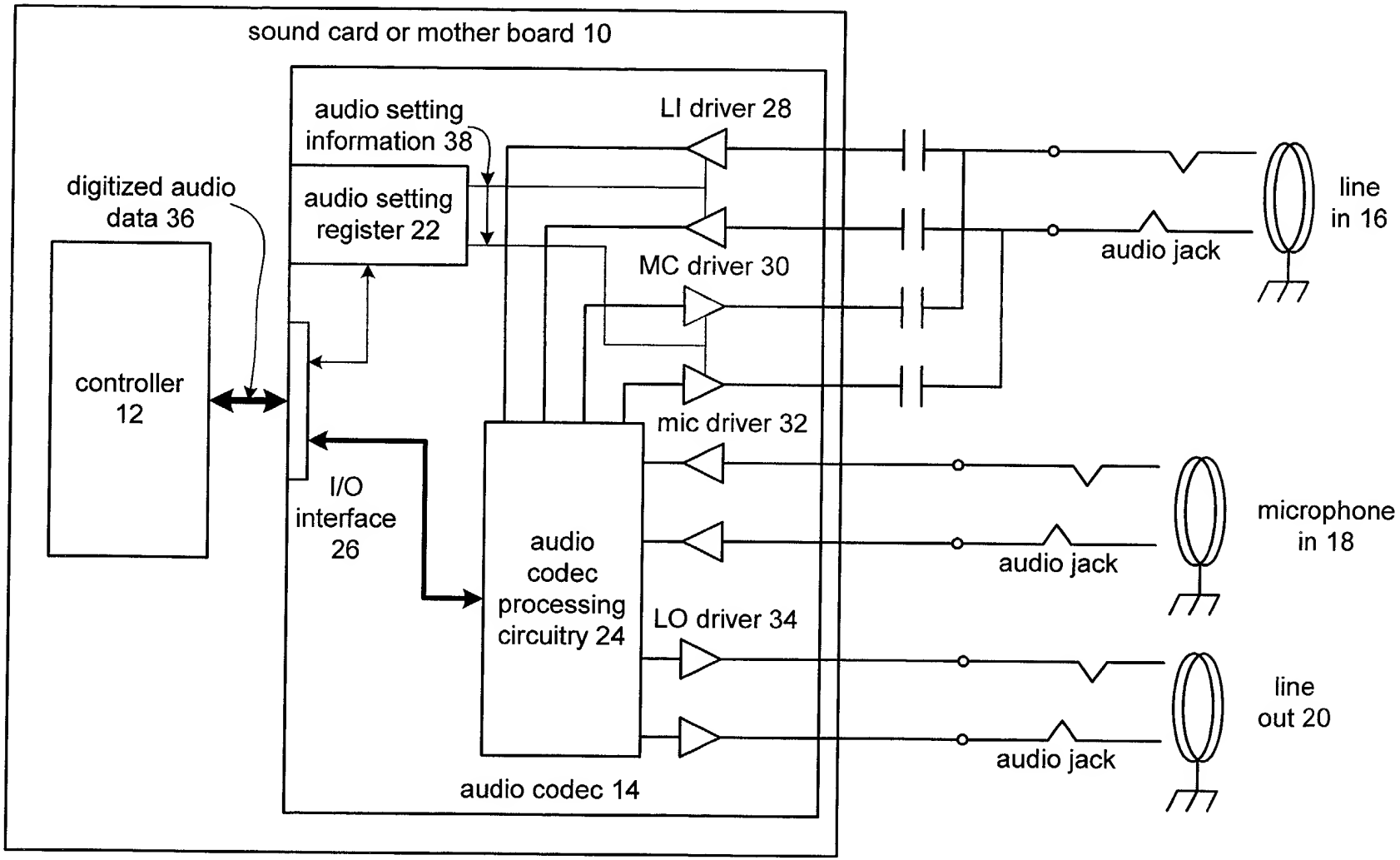
23. The audio codec of claim 21, wherein the memory further comprises operational instructions that cause the processing to disable the microphone driver by muting the line driver.

24. The audio codec of claim 21, wherein the memory further comprises operational instructions that cause the processing to disable the multiple channel driver by placing the multiple channel driver in a high impedance state.

METHOD AND APPARTUS FOR PROVIDING MULTIPLE CHANNEL AUDIO IN A COMPUTING SYSTEM

ABSTRACT OF THE DISCLOSURE

A method and apparatus for providing multiple channel audio in a computing system includes processing that begins by receiving an audio setup signal that indicates whether audio is to be outputted as stereo audio or multiple channel audio. When multiple channel audio is to be outputted, the line-in driver is disabled in the audio processing circuitry and the multiple channel driver of the audio processing circuitry is enabled. Thus, the multiple channel driver is operably coupled to the line-in audio jack. When the audio output is to be outputted as stereo audio, the multiple channel driver is disabled and the line-in driver is enable. Thus, the line-in driver is operably coupled to the line-in audio jack.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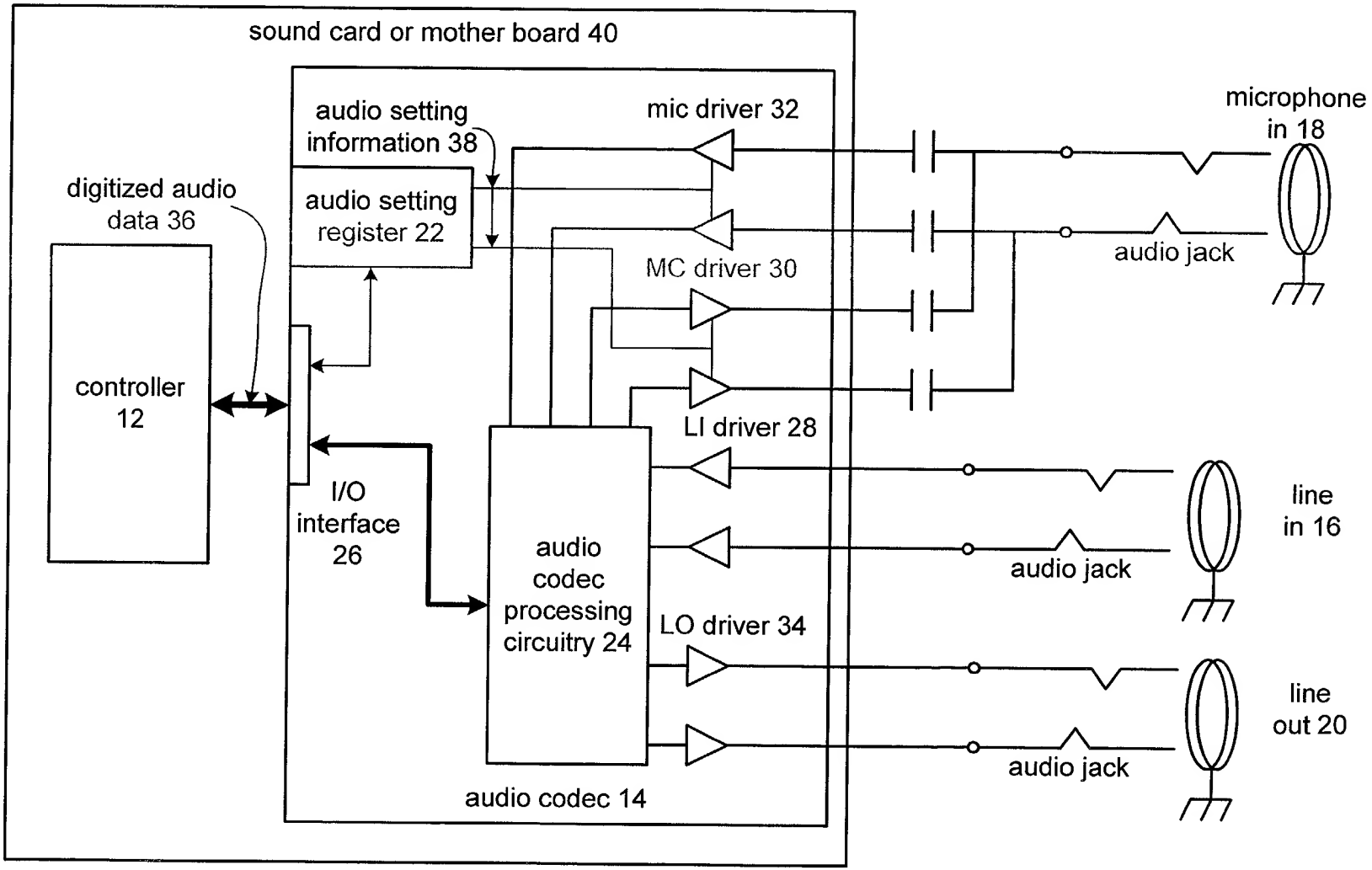
audio setting information 38
audio setting register 22
digitized audio data 36
controller 12
I/O interface 26
audio codec processing circuitry 24
audio codec 14
LI driver 28
MC driver 30
mic driver 32
LO driver 34
audio jack
audio jack
audio jack
line in 16
microphone in 18
line out 20

FIG. 1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audio setting information 38
audio setting register 22
digitized audio data 36
controller 12
I/O interface 26
audio codec processing circuitry 24
audio codec 14
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MC driver 30
LI driver 28
LO driver 34
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audio jack
line in 16
audio jack
line out 20
audio jack

FIG. 2

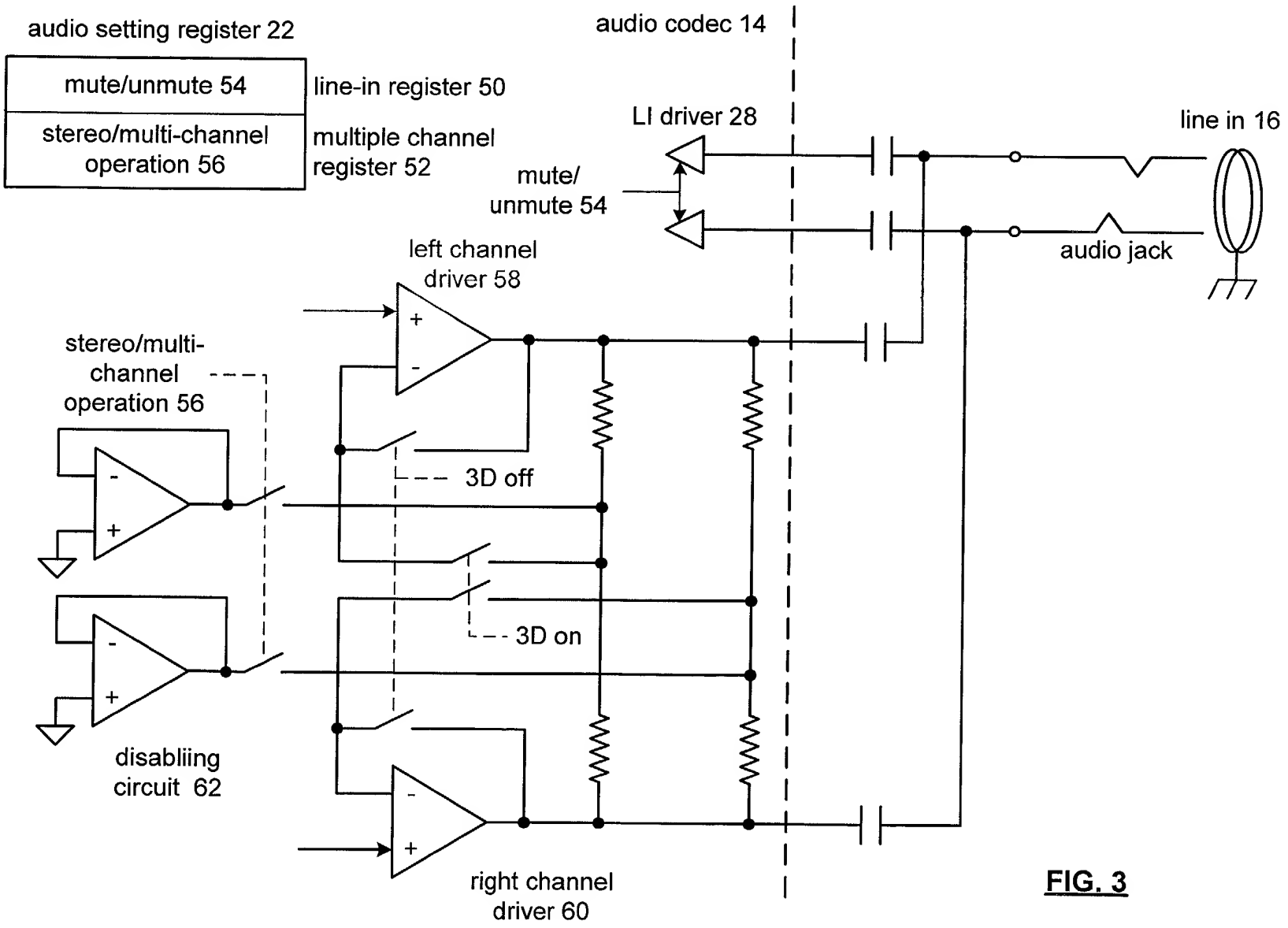

FIG. 3

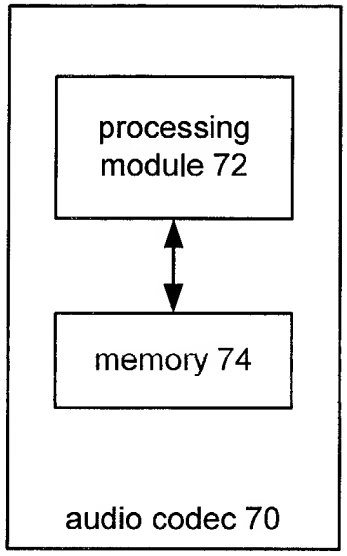

FIG. 4

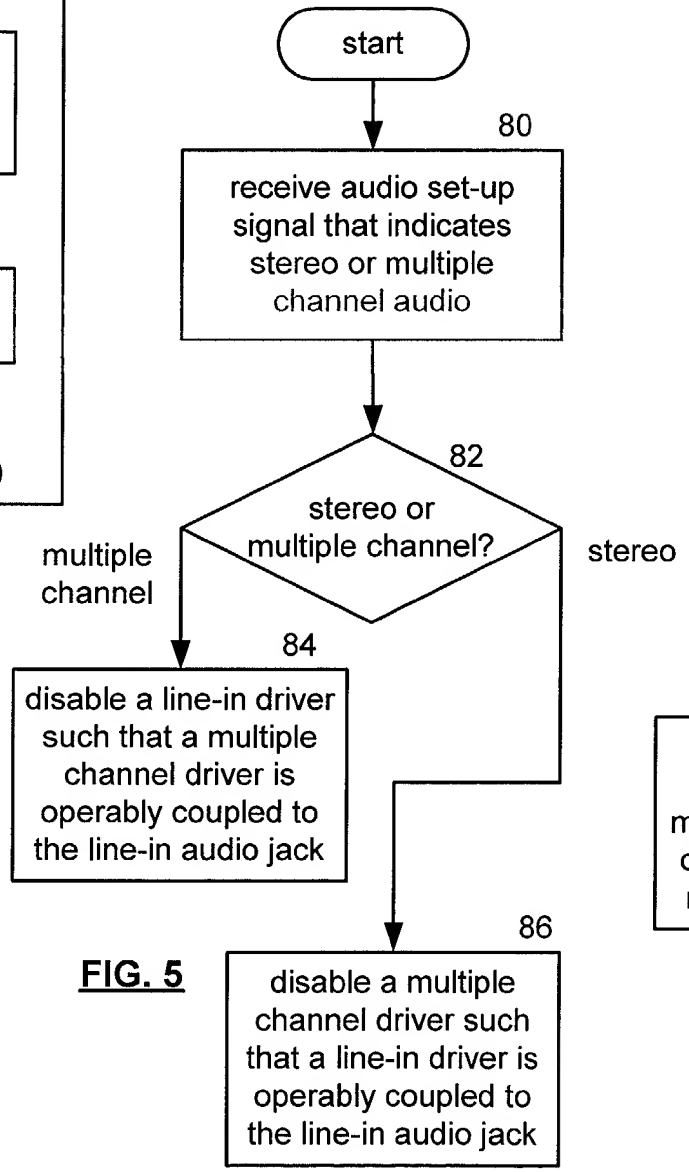

FIG. 5

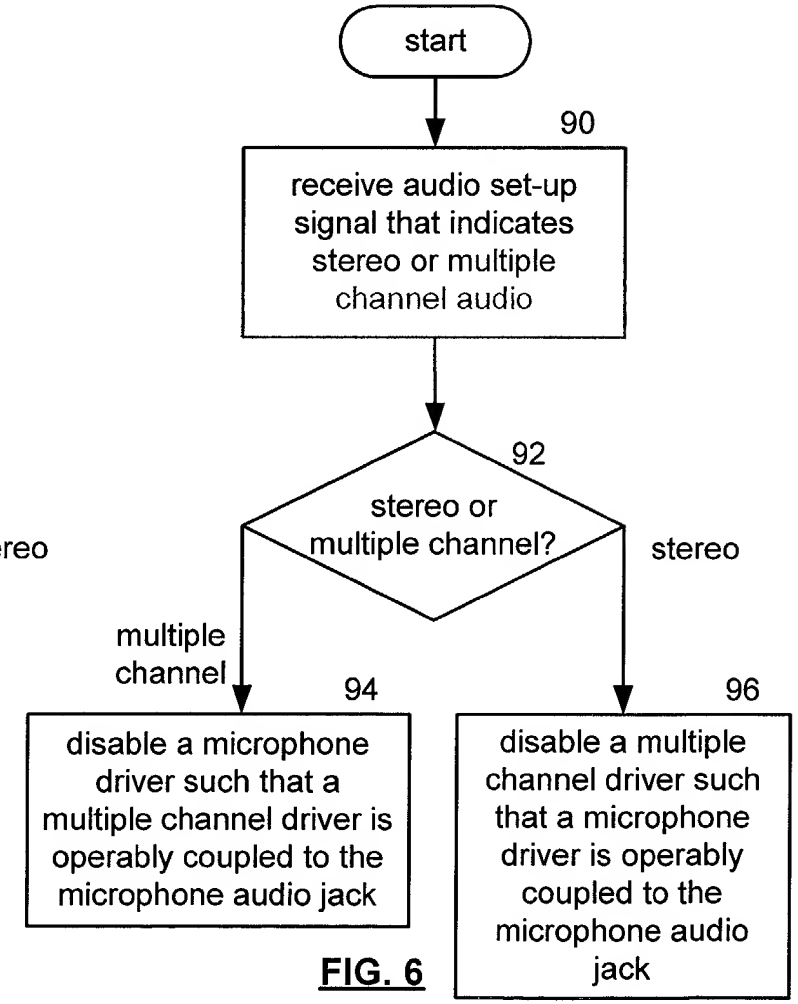

FIG. 6

PATENT APPLICATION
Docket No.: SIG000030

DECLARATION AND POWER OF ATTORNEY
Pursuant to 37 C.F.R 1.63 and 1.67

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name; and
I believe that I an inventor of the subject matter of a patent application entitled:

METHOD AND APPARATUS FOR PROVIDING MULTIPLE CHANNEL AUDIO IN A COMPUTING SYSTEM

The specification for the patent application (check one):

[X] is attached hereto.

[ ] was filed on as Application Serial No.
and was amended on (if applicable).

[ ] was filed as PCT International Application No. PCT/ on
and was amended on (if applicable).

[ ] was filed on as Application Serial No.
and was issued a Notice of Allowance on

I hereby state that I have reviewed and understood the contents of the above identified patent application, including the claims as amended by any amendment referred to above or as allowed as indicated above.

I acknowledge the duty to disclose all information known to me to be material to the patentability of this patent application as defined in 37 C.F.R. Section 1.56. If this is a continuation-in-part (CIP) application, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the Office all information known to me to be material to patentability of the application as defined in 37 C.F.R. Section 1.56 which became available between the filing data of the prior application and the national or PCT international filing date of this CIP application.

I hereby claim foreign priority benefits under 35 U.S.C. Sections 119 and 365 of any foreign application(s) for patent(s) or inventor's certificate(s) listed below. I have also identified below any foreign application(s) for patent(s) or inventor's certificate(s) filed by me or my assignee which: disclose the subject matter claimed in this patent application; and have a filing date that is either: (1) before the filing date of the application on which my priority is claimed; or, (2) before the filing date of this application when no priority is claimed:

Prior Foreign Patents
(list number, country, filing date MDY, date laid open, date granted or patented)

I hereby claim the benefit under 35 U.S.C. Sections 120 and 365 of any United States application(s) listed below and PCT international application(s) listed below:

Prior U.S. or PCT Applications

Application No.	Mo/Day/Yr Filed	Status

I hereby appoint Timothy W. Markison, Registration No. 33,534 of SigmaTel Inc., 2700 Via Fortuna, Sutie 500, Austin, Texas 78746 as my attorney, with full power of substitution and revocation, to prosecute this patent application and to transact all business in the United States Patent and Trademark Office connected therewith, and to file and prosecute any international patent applications filed thereon before any international authorities under the Patent Cooperation Treaty, and I hereby authorize him to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct them in writing to the contrary.

Please address all correspondence and direct all telephone calls to:
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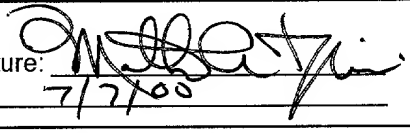
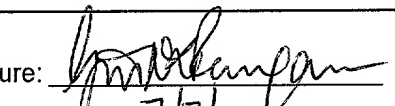
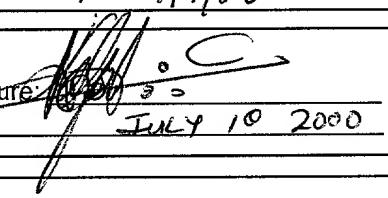
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this patent application or any patent issued thereon.

Inventor(s)

Rybicki Mathew A 10201 Kabar Trails Austin Texas 78759	citizen of: US	Signature:  Date: 7/7/00
Rangan Giri N. K. 9910 Jasmine Creek Drive Austin Texas 78726	citizen of: India	Signature:  Date: 7/7/00
Ifesinachukwa Kenneth G 2106 Lear Lane Austin Texas 78745	citizen of: US	Signature:  Date: JULY 10 2000
	citizen of:	Signature: _____ Date: _____
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	citizen of:	Signature: _____ Date: _____